PATENT ABSTRACTS OF JAPAN

(11)Publication number : 59-191368
(43)Date of publication of application : 30.10.1984

(51)Int.Cl. H01L 27/04
// H03K 13/02

(21)Application number : 58-065819
(22)Date of filing : 14.04.1983

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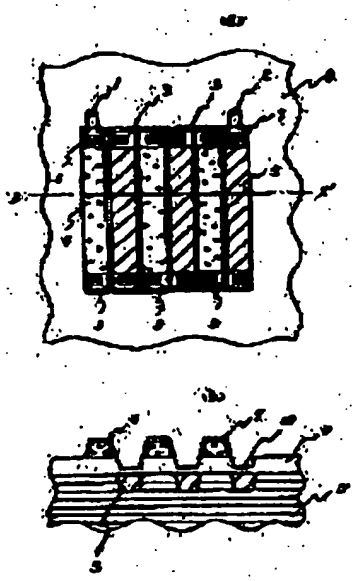
(54) SEMICONDUCTOR DEVICE

(57)Abstract:
PURPOSE: To reduce the area of a semiconductor device largely by combining a diffusion layer as a first resistor layer and a polycrystalline silicon layer as a second resistor layer.
CONSTITUTION: Polycrystalline silicon single body resistors 4 formed on a thick oxide film 8 shaped on a silicon substrate 11 through thermal oxidation, etc. are patterned by using photoetching technique, etc., and oxide films 9 are formed through thermal oxidation, etc. Diffusion unit resistors 5 are shaped through the diffusion of an impurity or ion implantation through thin oxide films 10. Openings for polycrystalline silicon contacts 6 and diffusion-layer contacts 7 are bored, and the polycrystalline silicon resistors 4 and the diffusion unit resistors 5 are connected mutually by lead-out conductors 1 and 2 and mutual connecting conductors 3, thus constituting the titled semiconductor device.



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[Date of request for examination]

[Date of sending the examiner's decision of rejection]

[Kind of final disposal of application other than the examiner's decision of rejection or application converted registration]

[Date of final disposal for application]

[Patent number]

[Date of registration]

[Number of appeal against examiner's decision of rejection]

[Date of requesting appeal against examiner's decision of rejection]

[Date of extinction of right]

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